11. (Amended) The semiconductor device according to claim 3, wherein at least two dummy lead wires are arranged in said semiconductor device and tip portions of two adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-3, 5, 6, 9, 11 and 13 are pending in the present application. Claims 4, 7, 8, 10, 12 and 14-27 have been cancelled and Claims 1-3, 5, 6, 9 and 11 have been amended by the present amendment.

In the outstanding Office Action, the drawings were objected to; the specification was objected to; Claims 1-27 were rejected under 35 U.S.C. § 112, second paragraph; Claim 1 was rejected under 35 U.S.C. § 102(e) as anticipated by Nakamura et al; Claims 1-3, 7 and 13 were rejected under 35 U.S.C. § 102(b) as anticipated by Oshino et al; and Claims 1-27 were rejected under 35 U.S.C. § 103(a) as unpatentable over Anjoh et al in view of the acknowledged prior art of Figure 1A.

In response to the objection to the drawings, the specification has been amended and enclosed is a separate letter requesting approval for changing Figure 3B as suggested in the outstanding Office Action. More specifically, the specification has been amended to recite "an opening portion 46" instead of "an opening portion 6" so the reference sign 6, which is not present in the figures, has been removed. Further, Figure 3B has been changed to show a cross sectional view of the line IIIB-IIIB shown in Figure 3A. Further, the specification has been amended at page 16, line 25, to recite a reference sign "46" instead of "6," and at page

17, line 24, to recite "a resin" instead of "the resin." No new matter has been added. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the rejection of Claims 1-27 under 35 U.S.C. § 112, second paragraph, Claims 1 has been amended as shown in the attached marked-up copy and is believed to comply with the requirements of 35 U.S.C. § 112, second paragraph, and Claim 4 has been cancelled. Accordingly, it is respectfully requested this rejection be withdrawn.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as anticipated by Nakamura et al. This rejection is respectfully traversed.

Amended Claim 1 is directed to a semiconductor device having at least a single dummy lead wire that is not electrically connected to a semiconductor element and does not include an outer lead portion for electrically connecting the semiconductor element to an external circuit of the semiconductor element. Further, the dummy lead wire is arranged in a space having at least twice a minimum pitch of an arrangement of lead wires.

For example, as shown in Figure 2A, the dummy lead wire 13' extends over a polyimide film 12, an opening 16, and the semiconductor device 11. This dummy lead wire 13' does not extend outward from the polyimide film 12 and therefore does not have an outer lead portion.

The present invention advantageously uses dummy lead wires not electrically connected to the semiconductor element so as to increase the total number of lead wires extended from the interposer to the semiconductor device and to permit the semiconductor element to be bonded to the resin molding with a high mechanical strength.[1]

Nakamura et al disclose in Figure 28 a semiconductor device having a dummy inner lead portion 5a formed by branching part of an inner lead portion 5a connected to a dummy

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[1]Specification, page 4, line 19 to page 5, line 4.

pad 6b.[2] Therefore, Nakamura et al disclose a dummy inner lead 5a connected to the semiconductor device through the bonding pad 6a and a bump electrode 7. However, Nakamura et al do not disclose the dummy inner lead portion 5a being arranged in a space having at least twice a minimum pitch of an arrangement of the lead wires. Accordingly, the inner lead portion 5a is electrically connected to the outer lead portion 5b in Nakamura et al, in contrast with the claimed invention where the dummy leads do not include an outer lead portion for electrically connecting the semiconductor element to an external circuit. Therefore, the semiconductor device in Nakamura et al does not achieve the same advantages as the present invention.

Accordingly, it is respectfully submitted Claim 1 and each of the claims depending therefrom patentably define over Nakamura et al.

Claims 1-3, 7 and 13 stand rejected under 35 U.S.C. § 102(b) as anticipated by Oshino et al. This rejection is respectfully traversed.

Oshino et al show in Figure 1 a semiconductor chip 3 having salient electrodes 4 and leads 5 secured to the semiconductor chip 3, and a dummy salient electrode 4A and dummy lead 5A provided to balance an arrangement of leads, to form resin uniformly and to improve a resin packaging property.[3] In Figure 1 there are two dummy leads 5A and 5B, with the dummy lead 5A electrically connecting to the semiconductor chip 3 through the dummy salient electrode 4A. Oshino et al does not teach or suggest that the dummy lead wire 5B electrically connects to the semiconductors 3 or any specific arrangement or space between the lead wires 5, and dummy lead wires 5A and 5B, as claimed in the present invention.

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[2]Nakamura et al, column 9, lines 16-27.

[3]See English translation of Oshino et al, first page.

Therefore, it is respectfully submitted Claim 1 and each of the claims depending therefrom also patentably define over Oshino et al.

Claims 1-27 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Anjoh et al in view of the acknowledged prior art of Figure 1A. This rejection is respectfully traversed.

Anjoh et al disclose a semiconductor device having a plurality of lead wires $3A_1$, $3A_2$, 3A and 3C. The plurality of dummy lead wires 3C are connected to the leads $3A_2$ together with lead wires 3A and form an integral part.[4] As disclosed in Anjoh et al at column 5, lines 10-17, the inner leads $3A_2$ are formed so that

> they can supply the power source voltage Vcc and the reference voltage Vss, respectively at any position on the active area of the semiconductor chip.

In other words, the dummy leads 3C, which are an integral part of the inner leads $3A_2$, are electrically connected to the power source voltage and the reference voltage.

Furthermore, Anjoh et al disclose the right side of the dummy lead wire 3C (the first wire 3A on the top and the last wire 3A on the bottom), shown in Figures 1, 3 and 4, is linked unitary to the left side, as shown in Figure 4, and each inner lead 3A has an outer lead 3B. The source voltage V_{CC} is applied to the right side via outer leads 3B (reference signs 1 and 14), the source voltage V_{SS} is applied to the left side via outer leads 3B (reference signs 15 and 28), and the lead wire $3A_{21}$ is "partly in contact with the chip 1."[5]

Thus, the dummy lead wire disclosed in Anjoh et al differs in structure from the dummy lead wire recited in amended Claim 1, since the claimed dummy lead wire "is not electrically connected to said semiconductor element and does not include an outer lead

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[4]Anjoh et al, column 5, line 57 to column 6, line 5.

[5]Id., column 5, lines 18-23.

portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element."[6]

Additionally, Anjoh et al do not disclose the dummy lead wires 3C being arranged in a space having at least twice a minimum pitch of an arrangement of the lead wires.

Figure 1A of the acknowledged prior art is asserted in the outstanding Office Action for its teaching of an insulating film 2 having an opening portion for accommodating the semiconductor element and serving to support the lead wires. However, Figure 1A of the acknowledged prior art does not teach or suggest what is also lacking in Anjoh et al, namely, at least a single dummy lead wire that is not electrically connected to the semiconductor element and does not include an outer lead portion for electrically connecting the semiconductor element to an external circuit of the semiconductor element, and the dummy lead wire being arranged in a space having at least twice a minimum pitch of an arrangement of the lead wires.

Accordingly, it is respectfully submitted Claim 1 and each of the claims depending therefrom also patentably define over Anjoh et al in view of Figure 1 of the acknowledged prior art.

Regarding the rejection of Claim 5, the combination of Anjoh et al and Figure 1A of the acknowledged prior art fails to teach dummy lead wires arranged in the semiconductor device and tip portions of two adjacent dummy lead wires, which have no lead wires in between, connected to each other.

Regarding the rejection of Claim 6, the combination of Anjoh et al and Figure 1A of the acknowledged prior art also fails to teach tip portions of the dummy lead wires positioned to face each other, connected to each other so as to form a straight single dummy lead wire.

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[6]Specification, Claim 1.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE SPECIFICATION

Please amend the specification as follows.

Please replace the paragraph bridging pages 16 and 17 as follows:

--On the other hand, a polyimide film 42 having a thickness of 75 μm is used as the interposer for supporting the chip 41 and holding a lead wire 43. The polyimide film 42 has an opening portion [6] 46 called a device hole. One end portion of the lead wire 43, which is formed of, for example, a copper foil, extends into the opening portion 46 so as to be connected directly to a connection electrode (pad) 44 formed on the surface of the chip 41 by a single point ILB (Inner Lead Bonding) method, with the other end portion of the lead wire 43 extending outward from the polyimide film 42.--

Please replace the paragraph bridging pages 17 and 18 as follows:

--A plurality of pads 44 are formed on the chip 41. However, the pads 44 are not arranged dense, but are arranged sparse. In the fourth embodiment shown in FIGS. 5A and 5B, the lead wires 43 are arranged in, for example, the four corner portions of the chip 41. In other words, the lead wires and pads are not arranged in the central portion of each side of the chip. Since the lead wire 43 serving to improve the bonding strength between the chip 41 and [the] a resin molding 45 is not arranged in the central portion in each side of the chip 41, cracks of the resin molding 45 tend to take place in the central portion in each side of the chip 41.--

IN THE CLAIMS

Please cancel Claims 4, 7, 8, 10, 12 and 14-27.

Please amend Claims 1, 2, 5, 6, 9 and 11 as follows:

--1. (Amended) A semiconductor device[,] comprising:

a semiconductor element;

a plurality of lead wires connected to a plurality of connecting electrodes of said semiconductor element;

at least a single dummy lead wire that is not electrically connected to said semiconductor element and does not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;

an insulating film having an opening portion for accommodating said semiconductor element and serving to support said lead wires connected to the connecting electrodes of the semiconductor element and said dummy lead wire;

said dummy lead wire is arranged in a space having at least twice a minimum pitch of an arrangement of said lead wires; and

a resin molding covering [the] a connecting portion between [the] tip portions of the lead wires and the connecting electrodes and [the] a tip portion of said dummy lead wire within the opening portion of said insulating film.

2. (Amended) The semiconductor device according to claim 1, wherein the tip portion of the dummy lead wire covered with said resin molding is positioned between [the] a peripheral portion of said opening portion and [the] a peripheral portion of the semiconductor element arranged within the opening portion.

5. (Amended) The semiconductor device according to claim 1, wherein at least two dummy lead wires are arranged in said semiconductor device and [the] tip portions of two

adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other.

6. (Amended) The semiconductor device according to claim 1, wherein said dummy lead wires are formed in two sides, which face each other, of said semiconductor element, and [the] tip portions of the dummy lead wires positioned to face each other are connected to each other so as to form a straight single dummy lead wire.

9. (Amended) The semiconductor device according to claim 2, wherein at least two dummy lead wires are arranged in said semiconductor device and [the] tip portions of two adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other.

11. (Amended) The semiconductor device according to claim 3, wherein at least two dummy lead wires are arranged in said semiconductor device and [the] tip portions of two adjacent dummy lead wires, which have no lead wires therebetween, are connected to each other.--